APPENDIX D

ESD TESTING

10. SCOPE

10.1 Scope. This appendix addresses ESD part testing, using the MIL-STD-883/MIL-STD-750 human body model test circuit as referenced by MIL-STD-1686. For informational purposes additional types of ESD testing such as the charged device model, field induced model, machine model, and charged chip model are discussed. Assembly and equipment level testing methodologies are also discussed. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-S-19500	-	Semiconductor Devices, General Specification for.
MIL-M-38510	-	Microcircuits, General Specification for.
MIL-H-38534	-	Hybrid Microcircuits, General Specification for.
MIL-I-38535	-	Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-750	-	Test Methods for Semiconductor Devices
MIL-STD-883	-	Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

20.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC)
801-2 - Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements.

(Application for copies should be addressed to the American National Standard Institute, 1430 Broadway, New York, NY 10018.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

30. ESD TEST MODELS

30.1 Human body model (HBM). People are prime sources of ESD damage, therefore the test circuit used in MIL-STD-1686, by reference to MIL-STD-883/MIL-STD-750, is based upon a human body model. Electrostatic charges generated by contact or rubbing materials (such as clothing) are readily transmitted to a person's conductive sweat layer causing that person to be charged. When a charged person handles or comes in close proximity to an ESDS part, the part may be damaged by direct discharge or by an electrostatic field. The ESD from a person can be reasonably simulated for test purposes by means of the MIL-STD-883 Method 3015 and MIL-STD-750 Method 1020 test circuit. These test circuits are also referenced in MIL-M-38510, MIL-H-38534/MIL-I-38535, MIL-S-19500 and have been widely used in the military and industry for ESD testing. The selected values for human body model capacitance (100 picofarads (pF)) and resistance (1,500 ohms) are not based upon a worst case model. Selection criteria for these values are discussed below.

Human capacitance may be as high as several thousand pF, but is typically 50 to 250 pF. A study performed on human capacitance indicated that approximately 80 percent of the population tested had a capacitance of 100 pF or less. The variation in human capacitance is due to factors such as variations in the amount and type of clothing and shoes worn by personnel, and differences in floor materials.

Human resistance can range from 100 to 100,000 ohms, but is typically between 1,000 and 5,000 ohms. The variation in human resistance is due to factors such as the amount of moisture, salt and oils at the skin surface, skin

contact area, and pressure. A value of 1,500 ohms provides a reasonable lower human resistance value. For energy sensitive parts, an increase in human body model capacitance to greater than 100 pF could result in damage to ESDS parts at voltage levels below those shown in MIL-STD-1686 appendix B. For instance, energy sensitive parts damaged at 400 volts using the 100 pF, 1,500 ohm human model would be damaged by slightly less than 300 volts had a 250 pF, 1,500 ohm model been used. Therefore, a part not considered as ESDS could actually be ESDS under more stringent human body model conditions. For predominately voltage sensitive ESDS parts, a variation in the capacitance value in the test circuit will cause little effect on the sensitivity. A decrease in the test circuit resistance will increase the voltage and energy delivered to the part and, therefore, the voltage level which causes damage decreases. The human body model of 100 pF, 1,500 ohms is considered to be a reasonable test circuit for standardizing the ESD sensitivity of parts.

Some ESDS parts are voltage sensitive while others are energy sensitive. In general, voltage sensitive parts fail due to dielectric breakdown of insulating layers or junctions. That is, the pulse shape, duration and energy can produce damage levels resulting in part thermal breakdown when the voltage level is below that needed to cause dielectric breakdown. The pulse is defined by the test circuit, the part resistance and capacitance (R-C) characteristics, the R-C time constant of the test circuit and the voltage at the capacitor. Thus, for a given test circuit with a fixed R-C (such as the MIL-STD-883 method 3015 test circuit) and a part with a given R-C, the voltage of the capacitor determines the shape of the pulse. Therefore, ESD sensitivity can be expressed as a voltage for both voltage and energy sensitive items for the given test circuit and part.

30.2 Charged device model (CDM). This model considers the case of a device that is charged on its lead frame or other conductive paths, and then quickly discharged to ground through one pin. In this case, charges residing on the metal parts of the die and package flow through the die and create failures of junctions, dielectrics and devices that are part of the discharge path. Device lead frames and packages can be charged triboelectrically just as the human body is charged. The voltage and the energy in such a device will depend on the position and orientation of the charged device with respect to ground.

The CDM sensitivity of a given device may be package dependent. Early experimental data indicates the same integrated circuit chip in a dual-in-line package (DIP) may be more susceptible to CDM damage when placed in a small outline package (SOP) or a pin grid array (PGA) package.

Experimental results indicate that the CDM discharge current is fast and oscillatory in nature, having both positive and negative polarities during the discharge, with risetimes measured in hundreds of picoseconds. By comparison, the HBM discharge has a typical rise time of 10-20 nanoseconds (ns) and

durations measured in hundreds of nanoseconds. The equivalent circuit that gives responses similar to a CDM discharge characteristic is effectively a series LCR resonant circuit. The inductance (L) represents the package lead frame inductance which can vary between 1 and 20 nanohenry (Nh), depending upon the type of package used. The CR portion is actually composed of several small capacitors in parallel, each in series with a resistor. Two equivalent circuit representations for this model are commonly used. One applies solely to bipolar devices and the other to MOS type devices.

Figure 3 is the equivalent circuit representation for bipolar devices. The model includes the device capacitance, inductance and resistance and some path contact resistance. Depending on its capacitance and the voltage it is charged up to, the device can store substantial amounts of energy to be released on contact with ground with average powers per pulse ranging from several hundred to several thousand watts. Such powers are sufficient to degrade device parameters or melt silicon, similar to the human body model case.

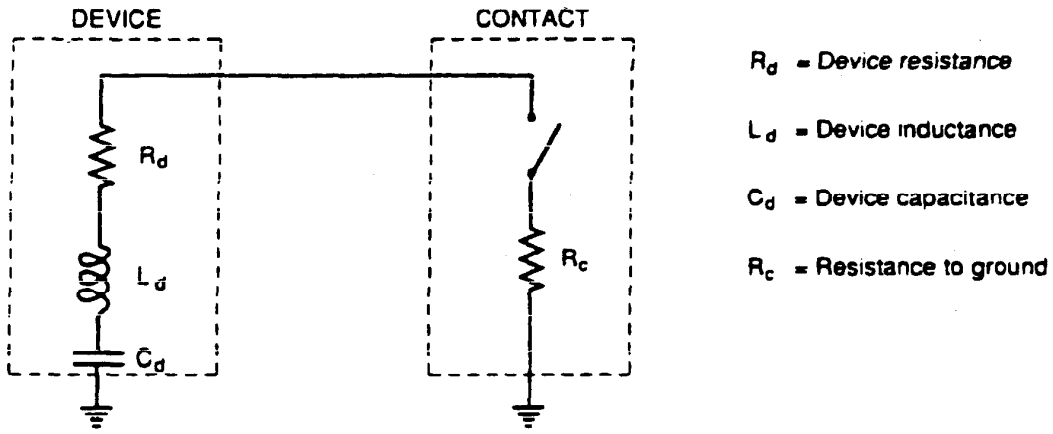


FIGURE 3. Equivalent circuit - bipolar devices.

The CDM MOS equivalent circuit is shown on figure 4. This model depicts multiple paths in the device with their own lumped elements. When one pin is grounded, each path on a device responds with its own characteristic discharge trace, and this leads to a potential difference between paths. If two such paths with significant differences in their discharge characteristics should cross or lie near each other, potentials exceeding the dielectric strength of the insulation between paths may occur with subsequent dielectric breakdown. In this model the charge is generated triboelectrically and resides on the

conductors of the device and package. The capacitance of a device is a variable, depending on device size, construction, and orientation to ground. Since the potential and stored energy vary inversely with device capacitance, given that the charge is constant, a reorientation of the device can either increase or decrease the device potential and energy.

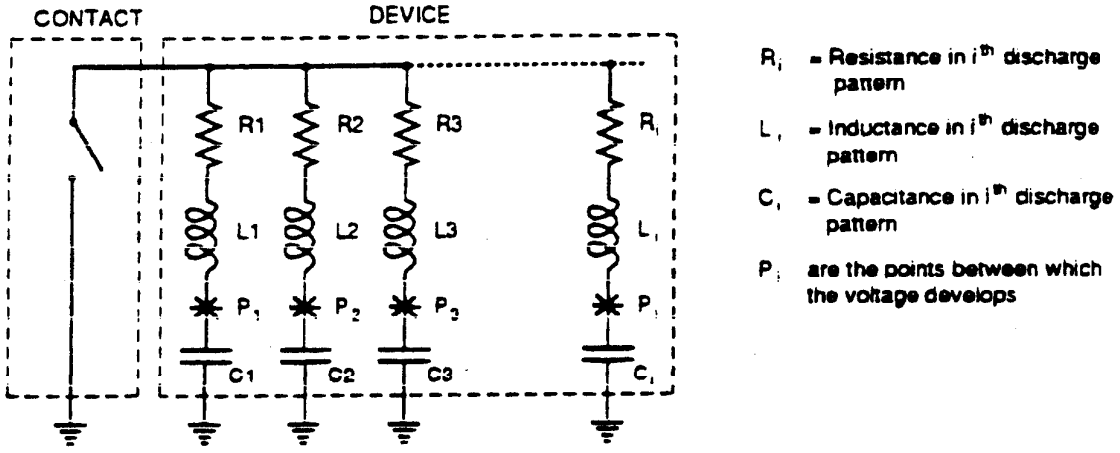


FIGURE 4. Equivalent circuit - MOS devices.

When devices on microcircuits are charged and inadvertently grounded, the energy in the discharge pulse is the sum of the energy stored on the device and on some of its connecting paths. The greater the energy the more potential for damage. Circuit boards with devices whose leads are routed directly to the terminals or edge of the boards are particularly susceptible to ESD damage during assembly and troubleshooting. These paths should be protected either by incorporating suitable path circuitry to shunt or reduce the discharge pulse power, or by using suitable ohmic edge board finger protectors to safely bleed the charge during handling.

In the case of HBM discharges, studies have revealed that damage is associated with metal penetration of junctions. This damage can be observed even when protective structures turn-on or function as designed. For CDM discharges, the current rise time is fast with an oscillatory waveform and protective structures may not have adequate time to function. Thus, CDM discharge can often be recognized because the damage occurs in the oxide (gate and field) areas. To ensure a high level of protection against the CDM discharge, it is necessary to have a large capacitance, with a small series resistance directly on the bond pad of the chip.

Gate oxides that fail in the charged device test are always near a pad, and either the gate or drain connection may lead to the pad. Analysis of charged oxide device test failures has led to some general design principles for avoiding oxide damage. Some design strategies are aimed directly at limiting the voltage across vulnerable gates. Most others indirectly limit the gate voltage through layout and voltage clamping of power and ground buses. As most of the package charge flows through these buses, there is the distinct possibility of excessive voltage excursions, which threaten thin gate oxides.

30.3 Field induced model. All devices will experience charge separation and discharge if placed in an electrostatic field and grounded. The field induced model simulates a situation in which a device is contacted to a ground source while in the presence of an electrostatic field, resulting in a high amplitude, short duration ESD transient. Figure 5 illustrates this concept using a dual in-line package (DIP) device. First, an uncharged device is placed in an electrostatic field causing a charge separation in accordance with electromagnetic field principals. If the device is then contacted to ground (or any body of sufficiently large capacitance), the resulting charge redistribution results in an ESD. Additionally, the device now has a net charge and, if it is removed from the electrostatic field, it is susceptible to damage from a charged device type of discharge. This illustration also assumes zero resistance to ground upon discharge.

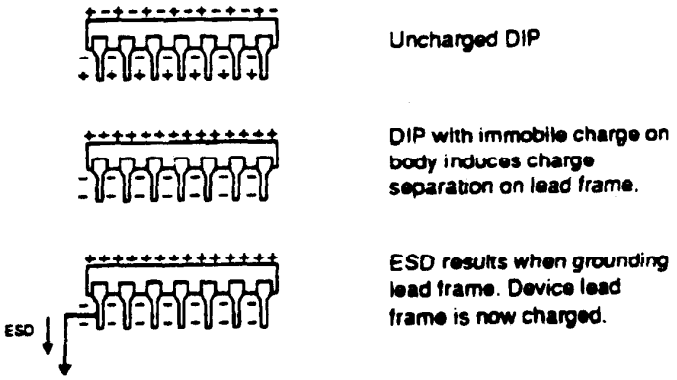


FIGURE 5. Charge induced on device.

30.4 Machine model. A variation of the HBM is the 200 Pf, zero-ohm machine model originated in Japan. This model represents the discharge occurring from the charged cables of a device or board tester. Test results using this model vary widely because series inductance is not specified. Some testers have

series inductance values of 150 millihenry (mH) or more, which limits current rise time.

30.5 Charged chip model. The charged chip model (CCM) represents the ESD damage that may occur in the chip pick up operation of the framed carrier process. The bare chip, divided to each of the devices on the isolation film, is picked up by the metallic collet. At this time, an ESD may occur between the chip and collet, because the electrical potential of the chip is high as a result of the electrostatic charges on the film. The discharge current, having a very fast rise time, flows into the chip through the collet. This transient high voltage is applied to the gate oxide film before the diode connect substrate to the gate oxides can respond and results in damage to the chip.

40. TYPES OF ESD TESTING

40.1 General. Testing methods are described in the following paragraphs. The test circuits of MIL-STD-883 Method 3015 and MIL-STD-750 Method 1020, as required by MIL-STD-1686, are applicable to ESD classification testing of parts, assemblies and equipment. Part failure is defined as the inability of a part to meet one or more of the electrical parameters of the part specification. When an electrical parameter has not been specified, a change of 10 percent or more of the parameter after testing voltage is applied should be considered a failure. However, any measurable change in a part electrical parameter, due to an ESD, could be an indication of part damage. In addition, ESD testing is considered to be destructive. Therefore, parts subjected to ESD testing shall not be used in deliverable hardware.

40.2 Latent defect testing. The susceptibility of ESDS parts to latent defects can be evaluated by methods such as the following. One method is a form of accelerated testing where ESDS parts are pulsed approximately 25 percent below their known voltage sensitivity levels with multiple discharges until failure occurs. Some ESDS parts are weakened by successive discharges and this weakened condition reduces part life. The use of multiple discharge testing is realistic since parts can be exposed to ESD pulses many times during their life, for example, during production, packaging, transportation, receipt inspection, kitting, assembly, and test. Another method is to subject a sample of parts to single or multiple discharges below their ESD voltage and energy sensitivity levels. Parts exhibiting performance characteristics within specification limits are then put on life test with a control sample not subjected to the ESD pulsing. It should be noted that use of elevated temperature to achieve accelerated life testing may result in healing of dielectric punctures caused by an ESD. Statistical evaluation of the lives of the two samples can be used to determine the effects of ESD latent defect failure mechanisms on part life. Another approach to the evaluation of latent defects can be based upon analysis of failures and historical trends where such data is available.

Damage due to discharge testing as provided above can be accumulative for some part types. Furthermore, an excessive repetition rate of discharges could build up hot spots in the part and cause an acceleration of the failure effects. Discharges should, therefore, be time spaced to allow for cooling within the part.

40.3 ESD spark testing. Most parts which are sensitive to ESD are also sensitive to other electromagnetic effects. Electromagnetic pulse (EMP) caused by ESD discharge in the form of a spark can cause part failure and cause equipment such as computers to upset. ESD spark testing can be performed by discharging the ESD in the form of a spark across a spark gap sized for the ESD test voltage. Another method is to bring the high voltage test lead of the test circuit close to the case or electrical terminal of an ESDS item, while it is operating.

40.4 Lot sample testing. Another consideration for ESD testing is to perform testing on lot samples of parts used in large quantities. Variations in lots from the same manufacturer, variations in fabrication techniques for specific date codes and variations between manufacturers, often result in differences in ESD sensitivity for the same part type. Lot ESD testing of parts on a sample basis could be used as a quality control check on purchased parts.

40.5 Assembly and equipment testing. The use of part testing procedures for an assembly and an equipment may be prohibitive in terms of costs. In such cases, classification techniques for assembly and equipment should be based on: (1) conservatively, the most ESDS part contained in that assembly; or (2) detailed circuit analysis of the voltage protection afforded by the ESD protective circuitry incorporated in that assembly or equipment. The MIL-STD-1686 Appendix C assembly and equipment test method is an adaptation of the MIL-STD-883 method 3015 HBM ESD test. MIL-STD-1686 Appendix C ESD testing applies only to assembly and equipment inputs, outputs, and interface connection points. This test method is used to determine compliance with MIL-STD-1686 design protection requirements. MIL-STD-1686 Appendix C testing is a destructive test and tested items shall not be used as deliverable hardware.

40.5.1 Assembly test method. Assembly testing is performed using a method and test circuit equivalent to that in MIL-STD-883 Method 3015. The following exceptions to the Method 3015 test apply: calibration and testing is required for 2,000 volts only; and the current waveform verification shall be accomplished at the output of the test apparatus (that is at the point of connection between the test apparatus and the assembly under test). A single assembly of each type shall be tested for ESD design protection at 2,000 volts using the following procedure. Prior to testing, the functionality of the assembly shall be characterized to verify it meets all applicable performance requirements. Each input, output, and interface connection point of the assembly shall then be pulsed with three positive and three negative pulses at a voltage level of 2,000 volts. Each connection point of the assembly shall

be individually and sequentially connected to terminal A of the test apparatus. The assembly ground or common should be connected to terminal B of the test apparatus. Upon completion of testing, assembly functionality shall be retested. Assemblies not meeting all applicable performance requirements, subsequent to testing, shall be classified as failed assemblies.

40.5.2 Equipment test method. Equipment testing is performed using a method and test circuit equivalent to that in MIL-STD-883 Method 3015. The following exceptions to the Method 3015 test apply: calibration and testing is required for 4,000 volts only; and the current waveform verification shall be accomplished at the output of the test apparatus (that is at the point of connection between the test apparatus and the equipment under test). Each equipment type shall be tested for ESD design protection at 4,000 volts using the following procedure. Prior to testing, the functionality of the equipment shall be characterized to verify it meets all applicable performance requirements. Each input, output, and interface connection point of the equipment shall then be pulsed with three positive and three negative pulses at a voltage level of 4,000 volts. Each connection point of the equipment shall be individually and sequentially connected to terminal A of the test apparatus. The equipment ground or common should be connected to terminal B of the test apparatus. Upon completion of testing, equipment functionality shall be retested. Equipment not meeting all applicable performance requirements, subsequent to testing, shall be classified as failed equipment.

40.5.3 Other test methods. There are other test methods available. One example is the International Electrotechnical Commission (IEC) Publication 801-2. It should be noted that the ESD test generator specified in this procedure uses a capacitance value of 150 pF and a discharge resistor value of 150 ohms.

APPENDIX E

DESIGN OF PROTECTION NETWORKS

10. SCOPE

10.1 Scope. This appendix provides information for the design of protection networks. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

30. INTRODUCTION

30.1 General. Various protection networks have been developed to protect sensitive electronic parts. These circuit protection networks provide limited protection against ESD. Many of the protection networks designed into MOS devices reduce the susceptibility to ESD to a maximum of 800 volts. MIL-M-38510 VZAP test voltages for CMOS, for example, vary from 150 to 800 volts. Protection circuitry of some devices is improving and protection to 4,000 volts appears to be achievable for some MOS devices. However, electrostatic potentials of tens of thousands of volts can be generated in uncontrolled environments.

30.1.1 Degree of protection afforded. The protection afforded by specific protection circuitry is limited to a maximum voltage and a minimum pulse width. ESDs beyond these limits can subject the part's constituents to damage, or the protection circuitry constituents themselves, which are also

often made of moderately or marginally sensitive ESDS parts may be damaged. Damage to the protection circuitry constituents could result in degradation in part performance or make the ESDS part more susceptible to subsequent ESDs. The degradation, for example, could be a change in speed characteristics of the ESDS part or an increase in leakage current of the ESDS part. Multiple ESDs, at voltages below the single pulse ESD sensitivity voltage or energy level can also weaken or cause failure of the part or protection circuitry constituents. Loss of protective circuitry may not be apparent after an ESD.

In summary, protection networks reduce but do not eliminate the susceptibility of a part to ESD. This reduction in ESD sensitivity, however, results in a lower incidence of ESD part failure.

The sensitivity of the same type of ESDS part can vary from manufacturer to manufacturer and from lot to lot by the same manufacturer. Similarly, the design and the effectiveness of protection circuitry also varies from manufacturer to manufacturer.

30.2 Protection network elements. The protection elements and their design parameters have to be optimized via an iterative procedure. The chosen design should be implemented, tested to failure, and the failure mode determined. Then a redesign to strengthen the failed structures can be undertaken, and the entire procedure repeated until the desired level of protection has been achieved. The optimization process starts with the analysis of established ESD protection elements, and design of ESD protection networks. The protection elements include diodes, resistors, contacts, metallization, three-layer devices (n-p-n or p-n-p), and four-layer devices (p-n-p-n) which are discussed below.

30.2.1 Diodes. Almost all "on chip" input protection networks employ some form of p-n junction. The factors that affect the characteristics of actual p-n junctions during ESD transients include high electric fields, high current densities, high temperature, and nonuniform current flow (second breakdown modes of operation), which will lead to significant deviation from the low voltage/low current diode characteristics. Consequently, the location of the p-n junction in a protection network is very important. It is imperative that circuit designers know the magnitudes of voltages and currents to be protected against. Furthermore, a clear understanding of the constraints on the breakdown voltage, input capacitance, area constraints, and the effects that an avalanching junction can have on nearby elements is required.

Recent advances in input protection circuit design for advanced CMOS processes include new process-tolerant circuitry based on a lateral silicon controlled rectifier (LSCR). The low-impedance, forward-conducting state provides design stability for a wide range of process variations. The LSCR device is very effective for various CMOS processes ranging from 2 μm abrupt junctions to 1 μm lightly doped drain (LDD) junctions with silicided diffusions. This

protection circuit can be designed into very-large-scale integration (VLSI) devices with CMOS processes. Latchup susceptibility of this device is not a problem since no direct connection is made to the positive power supply. Caution should be observed to prevent interaction between adjacent input pins. This can be achieved by employing preventive guard rings. The output ESD protection techniques for advanced CMOS processes include: (1) effective design and layout of CMOS buffers to achieve good ESD protection and (2), a new buried diffusion structure that is immune to ESD performance degradation with silicided processes. Because of the suppression of silicidation at the drain junction and the forming of an abrupt junction at the source/drain, this device has an excellent ESD performance for both human body and machine models.

30.2.2 Resistors. Resistors have been used in ESD protection networks for many years, and when properly employed, they can enhance the input protection capability of certain networks. Two major classes of resistors are the diffused and the polycrystalline silicon (poly) types. Studies have shown that protection networks employing poly resistors connected directly to the input bond pad were more susceptible than networks that used diffused resistors. Thus, if resistors are required as part of an ESD protection network, only the diffused type should be considered. Also, the layout of the resistor should avoid 90° turns or any other geometry that could result in non-uniform current and electric field distributions.

30.2.3 Three-layer devices (n-p-n or p-n-p). Three-layer structures are found in all integrated circuit technologies. As a result, the connections to these layers and the spacing between them can have a significant effect on the ESD susceptibility levels of input/output structures. These devices can be formed as a result of source/drain diffusions or when cross-unders and diffused resistors are placed close to each other. Since these parasitic bipolar transistor actions can be triggered by the avalanche breakdown voltage, it is desirable to have control over this voltage. One common way is to lay out parts of the drain junction as a spherical junction, or tailor its breakdown voltage by ion implantation. Also, punch-through and MOS transistor action can act as a trigger for parasitic bipolar action if these modes are controlled in such a way as to initiate significant impact ionization currents.

30.2.4 Four-layer devices (p-n-p-n). Probably one of the most important protection elements, as far as bulk CMOS and bipolar technologies are concerned, is the two-terminal four-layer device (p-n-p-n). In the discrete form, these devices are called thyristors or semiconductor controlled rectifiers (SCRs). In bulk CMOS or bipolar technologies, these four-layer structures are almost unavoidable. However, parasitic SCRs can be extremely effective in protecting against damage caused by ESD transients. With proper optimization of the parameters controlling the SCRs (the direct current

trigger voltage, holding current, and so forth), superior ESD protection networks can be realized.

To avoid the high field and/or current crowding regions associated with the p-n junctions, a novel on-chip ESD protection device using a static induction transistor principle is used. This method allows the sinking of discharge current directly from the pad to the substrate by implementing a vertical static induction transistor underneath each landing pad. This design avoids lateral flow of discharge current on the chip surface, and removes any reverse-biased junction along the discharge path. In addition, this saves chip area by being implemented under the contact pads, and offers the advantage of high speed and good thermal stability by virtue of being a majority-carrier device.

30.2.5 Contacts. Contacts between aluminum metallization and diffused regions play an important role in determining the ESD susceptibility levels of input structures. ESD hardness can be improved by allowing adequate metal-to-diffusion edge spacing; employing poly tabs for aluminum-poly-silicon contacts; the use of large circular contacts to avoid non-uniform current flow; and if process conditions allow, the use of deep diffusion junctions.

30.2.6 Metallization. A number of studies have shown that the dominant parameters for aluminum metallization failure during transient voltage conditions are the current density and the duration of the voltage pulse. For example, 90 degree turns cause nonuniform current distribution within the turn. Therefore, it is advantageous to avoid 90 degree turns in protection network metallization. Also, metallization at oxide steps may be much thinner than at other locations. Therefore, the widths of metal lines used in ESD protection networks should take into account this reduction in metallization thickness.

30.3 Design considerations for ESD protection networks. Protection network elements must always provide the lowest impedance path to ground for ESD transients, regardless of the pins receiving the transient, so that integral structures are never provoked into carrying the transient currents. The following are some general guidelines to implement protection networks.

(a) The network should defend against threats to all pin combinations.
(b) The network should defend against both polarities of the applied ESD transient.
(c) The design must be insensitive to slight misalignment and process variations.
(d) Use diffused resistors instead of poly resistors.
(e) Use poly tabs between metal-diffusion contacts.
(f) Avoid thin oxides on protection network elements.
(g) Allow adequate contact-to-diffusion edge spacing.

30.4 Design precautions. Various design techniques have been employed in reducing the susceptibility of parts and assemblies to ESD. Diffused resistors and limiting resistors provide some protection, but are limited in the amount of voltage they can handle. Zener diodes require greater than 5 nanoseconds to switch and may not be fast enough to protect a MOS gate. Furthermore, zener diode schemes, diffused resistors and limiting resistors reduce the performance characteristics of the part which in many instances are the primary considerations for which that part was designed.

30.4.1 Part and hybrid design considerations. Some design rules to reduce ESD sensitivity for parts and hybrids are as follows:

(a) MOS protection circuitry improvement techniques are: increasing diode size; using diodes of both polarities; adding series resistors; and utilizing a distributed network effect;
(b) Avoid cross-unders beneath metal leads connected to external pins; otherwise treat the part as electrostatic sensitive. Also, since cross-unders are diffused during the N+ (emitter) diffusion process, the oxide over the diffusion will be thinner, causing this area to have a lower dielectric breakdown. If a deep N diffusion step is used in the fabrication process, deep N diffusions, rather than N+ diffusions, should be used for cross-unders;
(c) MOS protection circuits should be examined to see if the layout permits the protection diodes to be defective or blown without causing the circuit to be inoperative;
(d) Distance between any contact edge and the junction should be 70 microns or greater on bipolar parts;
(e) Linear IC capacitors should be paralleled by a p-n junction with sufficiently low breakdown voltage;
(f) For bipolar parts avoid designs permitting a high transient energy density to exist in a p-n junction depletion region during ESD events. Use series resistance to limit ESD current or use parallel elements to divert current from critical elements. The addition of clamp diodes between a vulnerable lead and one or more power supply leads can improve ESD resistance by keeping critical junctions out of reverse breakdown. If a junction cannot be kept out of reverse breakdown, physically enlarging the junction will make it more ESD resistant by reducing the initial transient energy density in inverse proportion to its area;
(g) The protection of a transistor from ESD can be improved by increasing the emitter perimeter adjacent to the base contact. This lowers transient energy density in the critical emitter sidewall. Enlarging the emitter diffusion area also helps in some pulse configurations;

(h) As an alternative to using clamping diodes, which consume chip area and can cause unwanted parasitic effects, a "phantom emitter" transistor can be used to improve ESD resistance. The phantom transistor incorporates a second emitter diffusion shorted to the base contact. This creates a deliberate separation of the base contact from the normal emitter without interfering with normal transistor operation. The second emitter provides a lower break-down path BV_{CEO} between the buried collector and the base contact;

(i) Avoid pin layouts which put the critical ESD paths on corner pins which are prone to ESD;

(j) Avoid metallization cross-overs where possible. These cross-over areas are typically separated by thin dielectric layers. Cross-overs often impose a number of metallurgical requirements which are frequently incompatible. For example, once the first metallization layer (Al) is deposited, the circuit cannot be subsequently heated in excess of 550°C because the eutectic point of the Al-Si system is 575°C. Thus, the dielectric layer (SiO_2) should be deposited by a low temperature process such as pyrolytic deposition. This layer is prone to breakdown from ESD for two reasons:

(1) A low temperature growth of SiO_2 generally is not uniform in thickness and not free from pin holes;
(2) The dielectric layer is thin and thus the breakdown voltage is very low;

(k) Avoid parasitic MOS capacitors whenever possible. Microcircuits with metallization crossing over low resistance active regions, that is, V_{CC} over N+ guard rings are moderately sensitive to ESD. Such constructions include microcircuits with metallization paths over N+ guard rings. N+ guard rings are used in the N-type epitaxial islands to inhibit possible inversion of the N-type semiconductor to a P-type semiconductor, and to reduce the leakage current. Since the final oxide layer over the N+ guard ring is relatively thin, parasitic MOS capacitors of relatively low breakdown voltage are created when a metallization path passes over this ring. These MOS capacitor structures are ESDS as indicated in appendix B of MIL-STD-1686;

(l) Caution is advised in the use of microcircuits and hybrids containing dielectrically isolated bipolar parts which are generally moderately sensitive to ESD. Failure occurs due to breakdown of the thin dielectric layers between these small geometry bipolar parts from an ESD;

(m) The input protection network should be near the bond pad. In other words, bussing the electrostatic pulse around the chip should be avoided;
(n) Avoid metal to diffusion contacts. A short polysilicon strap of adequate width should be used to connect the aluminum to the diffused resistor;
(o) During the design of an electrostatic protection network consideration must be given to the entire path of the pulse.

30.4.2 Assembly design considerations. Procedures are as follows:

(a) Latchup in CMOS, with the exception of analog switches, can be avoided by limiting output current. One solution is to isolate each output from its cable line with a resistor, and clamp the lines to V_{DD} and V_{SS} with two high speed switching diodes. The use of long input cables poses the possibility of noise pickup. In such cases filter networks should be used;
(b) Additional protection can be obtained for on-chip protected or unprotected MOS by adding external series resistors to each input;
(c) Where practicable, an RC network consisting of a relatively large value resistor and a capacitor of at least 100 pF should be used for sensitive inputs on bipolar parts to reduce effects from ESD. However, if circuit performance dictates, two parallel diodes clamping to a half volt in either polarity can be used to shunt the input to ground. This reduces disturbances to the input characteristics;
(d) Leads of class 1 parts mounted on PWBs should not be connected directly to connector terminals without ESD protection. Assembly designs containing ESDS items should be reviewed for incorporation of protective circuitry;
(e) Systems incorporating keyboards, control panels, manual controls, or key locks should be designed to dissipate personnel static charges directly to chassis ground, bypassing ESDS parts.

30.4.3 Product design recommendations for ESD hardening. Different design recommendations apply for each failure mechanism.

(a) Direct Contact. Reduce the probability of direct contact by careful product design. Internal sensitive devices should be buffered with "robust" devices, high voltage clamping circuits, and/or filters before routing their signals to external parts or connectors. Where sensitive leads at connectors must be available to the outside world, they should be recessed and difficult or impractical to contact manually.

(b) Indirect Contact. An effective method is to provide for sufficient insulation or physical spacing between the outside world and any internal conductive parts or circuit traces which could lead directly, or indirectly, to an ESDS device. Insulation methods include installation of non-conductive films or tapes, sealing enclosure cracks or screw holes, and providing conductive guard traces or shields to divert the discharge energy from sensitive devices.

(c) Conducted or Radiated Noise. Careful choice of logic thresholds, shielding, low impedance circuitry, good ground system design, and meticulous circuit layout are some of the ways to minimize conducted or radiated noise problems. A conductive metallic barrier will tend to shield the circuits from radiated noise, especially if it completely encloses the circuits. But conductive coupling may occur due to secondary arcs from the shield to the circuits. To prevent this, the shield itself must be separated from the circuits. An insulating enclosure will not prevent radiated ESD noise from coupling to the circuits. Some enclosure designs utilize an insulating enclosure and within this, a metallic shield.

Compromising the integrity of most enclosures, for example, are holes, outlets for air and conductive items penetrating the barrier, such as screws, which allow ESD noise to pass through or around the barrier. These should be located well away from circuits. The noise through a hole is minimized by using several small holes instead of a single large one. Another approach is to make the depth of the hole at least five times its diameter, which greatly attenuates radiated ESD noise.

PCB design plays an important role in developing system immunity to ESD. The traces on a PCB are antennas for ESD-generated fields. Those connected to high impedance devices are antennas for electric fields, while those in low-impedance circuit loops are antennas for magnetic fields. To minimize the coupling to these antennas, line lengths must be kept as short as possible and loop areas must be kept as small as possible. Lines longer than a few centimeters and loop areas larger than a few centimeters square can receive significant ESD noise.

As the largest antennas within most systems, cables are particularly prone to having large voltages and/or currents induced in them by radiated ESD noise. But, cables can indirectly help prevent conductive coupling by providing a low-impedance path along which the charge may leave the system. The cable shield, the largest-diameter conductor in the cable, should be used as the ground path and be directly connected to a metal chassis.

Cables should be kept as short as possible, and each circuit line in the cable should be located physically close to its return line. In a ribbon

cable, for example, every signal line should have a ground line located next to it. The actions taken to reduce loop areas also minimize common-mode coupling.

Cable design sometimes utilizes the filtering concepts used in circuit design. Some cable connectors have built-in shunt capacitors or clamping suppressors, and others incorporate series ferrite inductive leads.

Often overlooked, firmware and software ESD solutions are powerful methods for reducing the severity of transient upsets such as system lockup.

(d) Induced Charge. A shield is recommended around the sensitive devices and their input leads to minimize induced charge effects of electrostatic fields. Low impedance circuitry and other noise reduction methods are also often effective for induced charges.

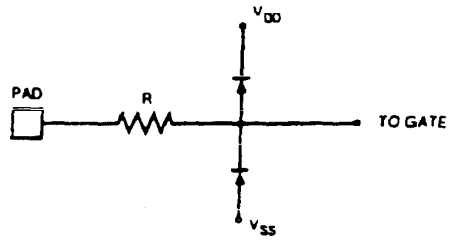
30.4.4 ESDS part protection networks. Manufacturers have incorporated protection circuitry on most MOS devices (see figure 6). The purpose of these protection networks is to reduce the voltage across the gate oxide below the dielectric breakdown voltage without interfering with part electrical performance. Differences in fabrication processes, design philosophies and circuitry have resulted in different gate protection networks.

30.4.5 Transient suppressors. Some transient suppressors, depending on the pulse width and shape, could reduce the voltage and energy flowing into an electrical circuit to levels sufficiently low to avoid damage to parts at the assembly levels.

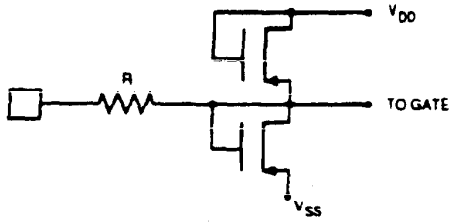
Two types of transient suppressors are commercially available. One is the metal oxide varistor; the other is a silicon p-n junction avalanche diode. Both rely on a nonlinear relationship between voltage and current such that at low voltages the current is extremely small, while at voltages above some "clamping" voltage the current increases rapidly. Both depend on the large voltage drop through the source impedance to reduce the voltage peak across the terminals of the device. The clamping voltage depends on the doping density in the p-n junction, and on the thickness (the number of grain boundaries) in the varistor. The junction area or volume (varistor) determine how much energy the suppressor can safely absorb during the transient. A highly desirable characteristic of these devices is the ability to respond in less than a nanosecond, as contrasted with the much slower response of air gaps and gas tube arrestors.

Suppressors include tin, zinc or bismuth oxide voltage-dependent resistors (VDRs), often referred to as metal oxide varistors, silicon voltage limiters, R-C networks and selenium stacks. Prior to making an ultimate judgment on any given type of suppressor, a final analysis should consider voltage levels to

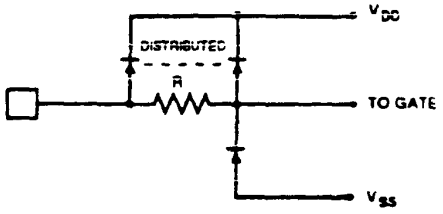
be encountered, response time of the suppressor, peak current, leakage current, energy absorption, operating temperature range, life, size, cost, and the voltage protection level desired.



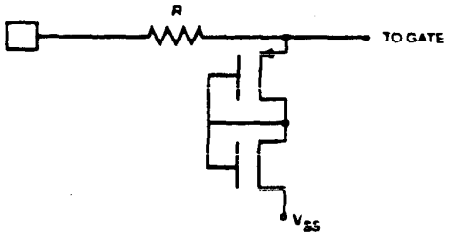
a. Diodes



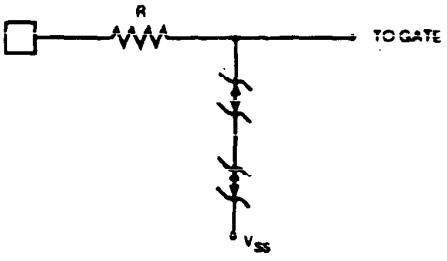
d. Transistors



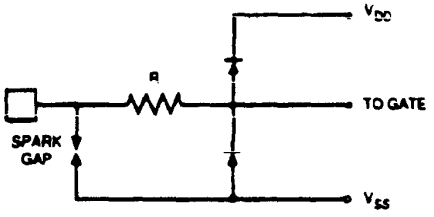
b. Distributed Diodes



e. Transistor Bilateral Devices



c. Zener Diodes



f. Spark Gap and Diodes

FIGURE 6. Gate protection networks.

30.5 Experimental studies. Results of some experimental studies on ESD protection networks are as follows:

(a) The most effective circuits for input protection for NMOS contains either a field oxide device or a diffusion diode/resistor. The field oxide device was found superior due to enhanced parasitic bipolar operation. An ideal diffusion diode/resistor was determined to be a large diffused diode to improve the power to area ratio and provide maximum heat dissipation followed by a long straight resistor.
(b) The ESD mean failure voltage of NMOS output buffers is a critical function of the buffer layout. Failure voltage exhibits an approximately exponential variation with source/drain window to gate spacing at small spacings and saturates above a critical spacing value. The number and distribution of source/drain contact windows are also important. Failure voltage generally increases with physical size of output transistors.
(c) Recently a new novel ESD protection device, Double Implant Field Inversion Device in Well (DIFIDW), with deep junctions and uniformly thick gate oxide designed for scaled CMOS VLSI high pin count chips has been developed.

APPENDIX F

PROTECTED AREAS

10. SCOPE

10.1 Scope. This appendix provides information on the concept, requirements, and operation of ESD protected areas. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-W-87893 - Workstation, Electrostatic Discharge (ESD) Control.

STANDARDS

MILITARY

MIL-STD-454 - Standard General Requirements for Electronic equipment.

HANDBOOKS

MILITARY

MIL-HDBK-419 - Grounding, Bonding, and Shielding for Electronic Equipments and Facilities Basic Theory.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

20.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

NATIONAL FIRE PROTECTION ASSOCIATION (NFPA)
70 - National Electrical Code.

(Application for copies should be addressed to the National Fire Protection Association, One Batterymarch Park, P.O. Box 9101, Quincy, MA 02269-9101.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

30. INTRODUCTION

30.1 Introduction. An ESD protected area consists of the tools, materials and equipment required to control or minimize static voltage levels. Complementing the requirement for protected areas are the associated handling procedures to be used in the protected area. The protected area can be a permanent designated area in a manufacturing, maintenance, or rework facility or a temporary area located immediately adjacent to equipment regardless of its physical location.

30.1.1 General concepts. The ESD protected area concept requires careful consideration of two elements. The first of these is to maintain personnel (electrical) safety at all times. This element is directly related to the types of materials (conductive or dissipative) selected for use in the protected area and the exact grounding procedures selected for use. The second element is related to the primary purpose of the protected area - the requirement to provide a technically adequate level of protection for ESDS items handled in the protected area. The objective of the protected area is to maintain the lowest possible electrostatic field intensity and voltages in the protected area.

The sophistication of the design of a protected area is directly related to the work processes performed, its location, and the environmental or physical limitations. For example, during field maintenance a protected area could consist of a temporary area free from static generating materials and equipped with a personnel wrist ground strap, portable protective work mat, and appropriate protective covering or packaging materials. A protective area in a manufacturing facility could include humidity controls, a comprehensive ESD

protective work bench constructed of protective materials and grounded appropriately, utilization of local or room air ionization, and conductive flooring with the associated heel grounders or conductive footwear.

The design of the protected area is directly impacted by the susceptibility of the item and the complexity of the handling procedures used in the protected area. As the protected area becomes more comprehensive, the handling procedures used in the protected area become less complex. Less comprehensive protected areas require handling procedures of increased complexity to ensure the desired levels of protection are provided. The relationship between the level of protection provided by the protected area and the protection provided by the handling procedures themselves entails a constant tradeoff between these two elements. Protected areas, may for simplicity, be designed to provide an equal level of protection for all ESDS items throughout a facility. This standardized approach requires that the level of protection selected be adequate to protect all items handled in a given facility. Alternatively, protected areas may be designed throughout a facility to provide the level of protection required only for those ESDS items handled at specific work locations. The first approach, that of standardized protective areas and handling procedures for a given facility may be the most desirable from the viewpoint of personnel training, program implementation and surveillance, and cost effectivity.

ESD protective materials and equipment are discussed in appendix I. The design and selection of materials for use in a protected area is at the option of the organization implementing an ESD control program. The information provided in this appendix and appendix I does not mandate or preclude the use of any specific materials or techniques. The materials or techniques selected should be technically adequate and cost effective.

30.1.2 Elements of a protected area. The protected area is the focal point for effective ESD controls. It should be noted that the protected area concept is intended for use only when ESDS parts, assemblies, and equipment are handled outside of their protective covering or packaging. ESDS material that is properly protected by technically adequate protective covering or packaging requires no unique handling or storage procedures as long as the protective covering or packaging integrity is maintained. Protected area concepts consist of various complementary elements which include:

(a) Grounding considerations
(b) Safety and grounding requirements
(c) Tools, materials and equipment
(d) Operating procedures

Each of these elements is discussed below.

40. GROUNDING CONSIDERATIONS

40.1 General. ESD protective materials and equipment that are to be grounded should be attached to the earth electrode subsystem of the facility (see MIL-HDBK-419) or attached to a ground constructed and tested in accordance with NFPA 70. Grounding on military platforms such as shipboard, aircraft or other vehicles shall be in accordance with the applicable military requirements, standards, or specifications.

50. SAFETY AND GROUNDING REQUIREMENTS

50.1 Personnel safety. Of prime importance are personnel safety requirements. The safety requirements of MIL-STD-454, Requirement 1 should be considered in the construction of ESD protected areas to reduce the chance of electrical shock to personnel. Maximum current levels in ESD protected areas should be limited to the perception level as shown in MIL-STD-454, requirement 1.

50.2 Ground potential of electrical equipment and power tools. The design and construction of the ESD protected area and ESD grounded work benches should ensure that all external parts, surfaces, and shields in electronic test equipment and power tools are at a common ground potential at all times during normal operation. The design should include consideration of potential ground faults and hazardous voltage levels which may exist in the protected area. Tools and test equipment on grounded work benches with metal or other conductive coverings can shunt the protective resistance in the work bench ground cable if allowed to contact the work surface. As an added precaution for personnel safety ground fault circuit interrupters (GFCI) can be used with electrical equipment. The GFCI senses leakage current from faulty equipment and interrupts the circuit almost instantaneously when these currents reach a potentially hazardous level. CAUTION MUST BE OBSERVED IN EMPLOYING PARALLEL PATHS TO GROUND THAT COULD REDUCE EQUIVALENT RESISTANCE OF PERSONS TO GROUND TO UNSAFE LEVELS. Personnel movements in conjunction with wrist straps, table tops and floor mats could result in such parallel paths.

50.3 Ground potential of protected areas. Grounded work bench surfaces constructed of metallic materials such as stainless steel require careful design and evaluation in the context of personnel electrical safety.

50.4 Alternative grounding procedures. There are many alternative grounding techniques that may be suitable for use in providing ESD protection. Selected grounding techniques must provide personnel safety at all times and be in accordance with the National Electrical Code and all other applicable requirements.

50.5 Grounding tradeoffs. The exact grounding methods selected for use in a given facility involve a series of technical tradeoffs predicated upon the

exact materials selected for use and their relationship to the organizations' ESD handling procedures. The methodology and techniques selected must not compromise personnel safety. The use, or non-use of current limiting resistors in grounding circuitry is intimately related to the material selected for ESD protective work surfaces (which can range from metallic conductors such as stainless steel to dissipative material with surface resistivities of up to 10^{12} ohms per square). Other factors which are unique to each organization and facility, include the exact type of work performed in each protected area, that is, electrical test, mechanical assembly, and so forth, and the potential voltage sources that may be present in the protected area. The use, or non-use of devices such as GFCIs also requires careful consideration. Each of these elements preclude the design of a protected area which would be universally acceptable to all users.

60. TOOLS, MATERIALS AND EQUIPMENT

60.1 General. The tools, materials and equipment selected for use in a protected area can range from the minimum such as ESD protective work bench surfaces and personnel wrist straps, to more complex configurations that include air ionization, protective flooring, and continuous monitoring of wrist strap integrity and static voltage generation. The items selected are at the option of the protected area designer, however, care should be exercised during the design, construction and use of the protected area to exclude prime charge sources (see Appendix A, Table III). Figure 7 illustrates an ESD work bench. In addition, the protected area should be identified by precautionary signs; for example, ESD PROTECTED AREA. Figure 8 is an example of an ESD protected area sign and figure 9 is a typical certification/reinspection label. Information on ESD protective materials and equipment is contained in Appendix I.

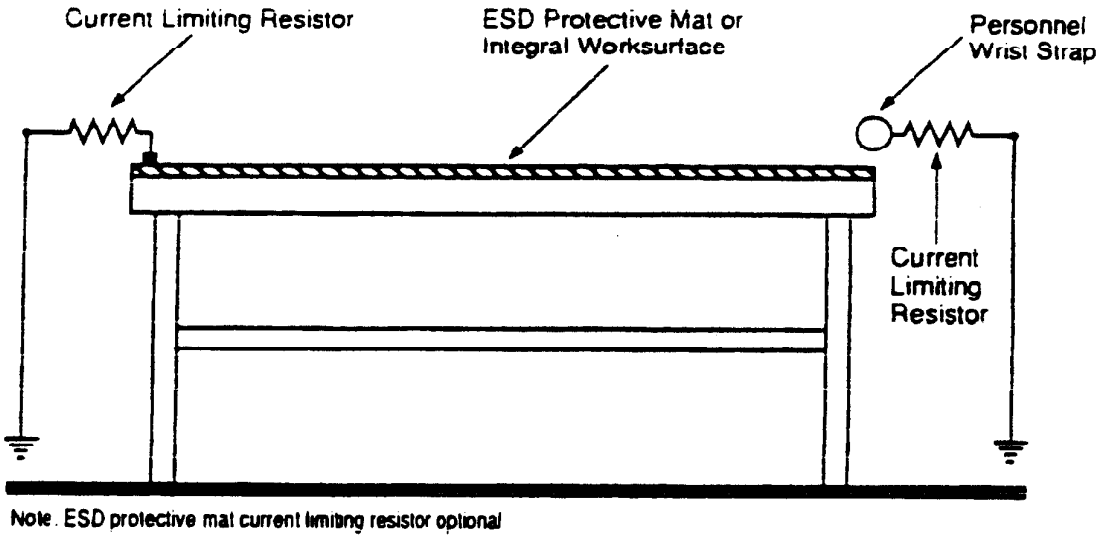


FIGURE 7. ESD protective work bench.

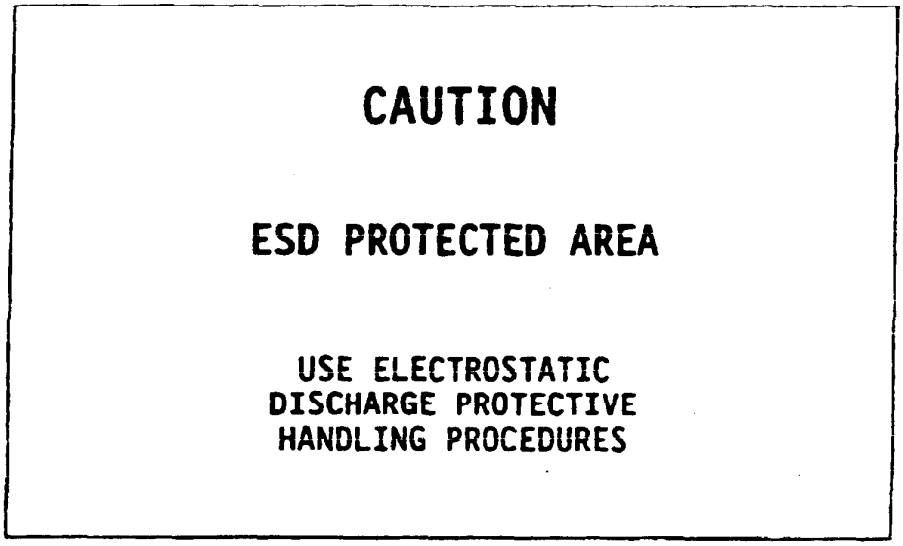


FIGURE 8. ESD protected area caution sign.

Certification Date: _____

By: _____

Reinspection due: _____

FIGURE 9. ESD protected area certification/reinspection label.

60.2 Military specifications. MIL-W-87893(3D) has been prepared by the Department of the Air Force principally for Air Force use. This specification covers specific resistance values, static decay values, and general construction requirements for static control workstations and their components.

70. OPERATING PROCEDURES

70.1 General. Access to ESD protected areas should be limited to personnel who are properly trained (see appendix J). General guidelines and sample operating procedures for use during handling of ESDS items may be found in appendix H.

80. CERTIFICATION/VERIFICATION AND MONITORING OF PROTECTED AREAS

80.1 Certification/verification and monitoring. Certification and monitoring should be performed at the time of installation for permanent protected areas and periodically thereafter. Certification takes place to ensure the protective area is installed as designed. Verification or periodic monitoring ensures the continuous integrity of the protective area.